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STEELMAN, MARY J	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/819,351	Applicant(s) WATANABE, KATSUMI	
	Examiner Mary J. Steelman	Art Unit 2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/28/01,1/2/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *#2,#4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-6 are pending.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. IDS received 28 March 2001 has not been considered. Documents are in Japanese. In reference to IDS received 02 January 2004, only the Abstract has been considered. Document is in Japanese.

Drawings

4. FIG. 8 is missing a description for 'S8' in the Specification.

Specification

5. Examiner objects to the length of the Abstract. Abstract should be limited to 150 words. See:

Content of Specification

(j) Abstract of the Disclosure: See MPEP § 608.01(f). A brief narrative of the disclosure as a whole in a single paragraph of 150 words or less commencing on a separate sheet following the claims. In an international application which has entered the national stage (37 CFR 1.491(b)), the applicant need not submit an abstract commencing on a separate sheet if an abstract was published with the international application under PCT Article 21. The abstract that appears on the cover page of the pamphlet published by the International Bureau (IB) of the

World Intellectual Property Organization (WIPO) is the abstract that will be used by the USPTO. See MPEP § 1893.03(e).

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors.

Claim 1 logic is unclear (page 23, lines 6-11): "...upon detecting that the instruction address/instruction code data...matches one of a predetermined instruction address and predetermined instruction code set as an event condition..." (Implies match either (1) a predetermined address or (2) a predetermined instruction code set as an event condition...")

Claim 1 is logic is unclear (page 23, lines 12-25):

Generate trace data if:

IF Branch instruction OR start signal is active

Then output uncompressed instruction address as trace data

(Delete 'AND' on line 17?)

IF NOT branch instruction AND signal NOT active

Then generate compressed instruction addresses

AND combine compressed instruction addresses

AND output compressed instruction addresses as trace data

Claim 4 logic is unclear: See page 26, lines 36-37, "and OR..."

Claim 5 logic is unclear: See page 26, lines 7-8, "and said OR means..."

Claim 6 logic is unclear: See page 27, "...storing an...address that has traced a program..." (an address that was traced in a program? Or an address that has traced a program?)

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over 5,535,331 to Swoboda et al., in view of US Patent 5,764,994 to Craft..

Per claim 1:

-a CPU (Central Processing Unit) for executing a target program and outputting instruction

address/instruction code data; (Swoboda: Col. 6, lines 41-43, "Simulator executes a software program that simulates operation of the target chip for cost-effective software development and program verification..." See fig. 44.)

-event management means for asserting and outputting a section trace start signal upon detecting that the instruction address/instruction code data from said CPU matches one of a predetermined instruction address and predetermined instruction code set as an event condition in advance; (Swoboda: Col. 6, lines 57-64, "Simulator execution modes include...While Condition Exists...Trace expressions are readily defined. In trace execution, display choices include 1) designated expression values...Breakpoint conditions include..." Events are set as conditions or breakpoints.)

-trace data generation means for, when an instruction code of the instruction address/instruction code data from said CPU is a branch instruction, or the section trace start signal from said event management means is active, outputting an uncompressed instruction address as trace data, and when the instruction address of the instruction address/instruction code data is not the branch instruction, and the section trace start signal is not active, generating a plurality of compressed instruction addresses by compressing the instruction address of the instruction address/instruction code data, and then combining the compressed instruction addresses and outputting the compressed instruction addresses as the trace data; (Swoboda, Abstract, lines 1-3, "Operations of a data processing device are traced (trace data generation means) by detecting a jump address (detecting branch address an event) in the program counter sequence, and pushing

the jump address onto a trace stack. (assert start signal)", col. 7, lines 18-21, "A trace memory is also displayable. A record of the simulation session can be maintained in a journal file so that it can be re-executed..."

Swoboda failed to disclose details related to the choice of compressing or not compressing certain data prior to storing. However, Craft disclosed (col. 3, lines 15-35, "With reference now to FIG. 2, there is illustrated a high-level logic flow diagram of a method for compressing a set of compiled microcode...an address location of each branch instruction within this set of compiled microcode may be identified...This set of compiled microcode is then parsed into...segments...Each of these microcode segments begins after an identified branch instruction...Subsequently each of these microcode segments is individually compressed..." Col. 3, lines 53-55, "the microcode compression is basically dictated by the branch points and entry points within the set of compiled microcode..." Col. 4, lines 42-44, "...all compressed microcode segments are concatenated (combined) by special linker..."

-a trace memory for storing the trace data from said trace data generation means. (Swoboda, col. 8, lines 35-42, "Emulator controller card provides full-speed execution and monitoring of each target chip...breakpoints, software and hardware trace and timing, and single step execution are provided...Program data and program memory can be uploaded (store trace memory) or downloaded.)

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified Swoboda's processor tracing device, to include a technique to

compress certain parts of the code, as disclosed by Craft because (Craft, col. 2, lines 11-12), "By doing so, the required memory for storing the compressed executable microcode (the traced data) is reduced."

Per claim 2:

-said event management means keeps a data latch signal active during a predetermined period and outputting the data latch signal, (Swoboda: Col. 10, lines 42-43, "...bits that define control operations (like commands or instructions) available through controller card." Col. 10, lines 50-53, Shift register latches (SRLs) designated "S" are distributed through the device like a string of beads on a serial scan path...to provide access to all important registers." Col. 10, lines 65-67, "Emulation adapter in different forms involves hardwired state machine circuitry (data latch signals)...or microcoded state machine embodiments.")

-said trace data generation means receives the instruction address,/instruction code data from said CPU and the section trace start signal from said event management means and, when the data latch signal from said event management means is active, latches the instruction address/instruction code data. (Swoboda: Col. 9, lines 1-14, "Software breakpoints allow program execution to be halted at a specified instruction address (trace start signal)...When a given breakpoint is reached, the program either halts execution to permit user observation of memory and status registers, or the breakpoint is included in a more complex condition (receive address/code data & trace start signal & data latch signal is active...), which when satisfied

results in an appropriate stop mode being executed (latch instruction address/ instruction code data)...This information is suitably saved on command in a file for future analysis...")

Per claim 3:

-event setting means in which event setting data containing the predetermined instruction address/instruction code as the event condition and the active period of the data latch signal are set in advance, (Swoboda, col. 10, lines 42-43, "...bits that define control operations available through controller card..." and lines 50-53, "Shift register latches (SRLs) designated "S" are distributed through the device...to provide access to all important registers...")

-event detection means for, upon detecting that the instruction address/instruction code contained in the event setting data output from said event setting means matches the instruction address/instruction code of the instruction address/instruction code data from said CPU, asserting and outputting the section trace start signal and asserting the data latch signal during the active period set in said event setting means and outputting the data latch signal. (Swoboda: Abstract, lines 1-3, "Operations of a data processing device are traced by detecting a jump address in the program counter sequence, and pushing the jump address on to a trace stack." Col. 11, lines 26-41, "The instruction register can receive serial scan signals...MUX...can select the output signal from the instruction register or from another MUX..." Col. 32, lines 51-55, "...the preferred embodiment sets up a condition in the analysis domain, and then the analysis domain effectively monitors the chip as it runs in real time, then detects when the condition occurs...")

Per claim 4:

-instruction address/instruction code latch means for latching the instruction address/instruction code data from said CPU during the active period of the data latch signal and outputting the instruction address/instruction code, (Swoboda, col. 11, lines 26-41, "Test access port (TAP) controller is in turn coupled to instruction register (IR) and a first multiplexer. The instruction register can receive serial scan signals from the TDI line and output serially to MUX. MUX is under control of the TAP and can select the output signal from the instruction register or from another MUX. The instruction register also controls a bypass register (BR) and one or more boundary scan registers (BSR). The bypass register receives the TDA signal and outputs it to MUX. MUX is under control of the instruction register. Based on the instruction loaded into the instruction register, MUX outputs its input from the bypass register or its input from one or more BSRs..." Col. 14, lines 2-6, "Analysis circuitry is connected to the CPU core as described more fully herein. The analysis circuitry includes condition sensors such as hardware breakpoint sensors for the controlled stops and trace stack circuitry for real-time trace recordkeeping..." Col. 31, lines 45-52, "Memory operations are suitably generated using CPU resources. Memory accesses are generated by scanning in a CPU state including appropriate CPU memory access instructions, which causes memory accesses to be generated to the appropriate memory or I/O space. This is accomplished by loading a machine state with the pipe flush bit set, and appropriate instruction in the pipeline to cause the desired memory operation.")

-instruction address data compression means for, when a received uncompressed data selection signal is active, outputting the instruction address from said instruction address/instruction code

latch means as the compressed instruction address, and when the uncompressed data selection signal is not active, outputting difference data obtained by subtracting an immediately preceding instruction address from a current instruction address as the compressed instruction address,

Swoboda failed to disclose details on compression and an active / inactive signal. However, Craft disclosed (col. 3, lines 30-35), "...segments begins after an identified branch instruction or at a target address of an identified branch instruction and ends just before another branch instruction...each of these microcode segments is individually compressed...")

-branch instruction determination means for determining whether the instruction code from said instruction address/instruction code latch means is the branch instruction, and upon determining that the instruction code is the branch instruction, asserting and outputting a branch instruction detection signal, (Swoboda: col. 3, lines 29-31, "...including a semiconductor chip, an electronic processor on-chip and an on-chip condition sensor (determine if branch instruction) connected to the electronic processor for analysis (output signal) of the operations." Col. 6, lines 51-53, "Simulation parameters are quickly stored/retrieved from files to facilitate preparation for individual sessions..." Col. 6, lines 57-64, "Simulator execution modes include...While Condition Exists...Trace expressions are readily defined. In trace execution, display choices include...expression values...Breakpoint conditions include..." Conditions can be set to determine a branch instruction.)

-trace control means for, when the received uncompressed data selection signal is active, outputting the compressed instruction address from said instruction address data compression means as trace data, and when the uncompressed data selection signal is not active, combining a plurality of continuously received compressed instruction addresses in accordance with a bit width of said trace memory and outputting the combined instruction addresses as the trace data, and outputting a trace data write signal for instructing said trace memory to write the trace data and a trace memory address for designating a storage address of said trace memory, (Swoboda: Col. 34, lines 42-46, "CPU core is further improved by providing a trace stack circuit distinct from program counter stack. Unlike stack, trace stack circuit develops a history (write the trace history to storage) of program counter discontinuities..." Col. 7, line 19, "...session can be maintained in a journal file (memory)...")

Swoboda failed to disclose details on compression and an active / inactive signal. However, Craft disclosed (col. 3, lines 30-35), "...segments begins after an identified branch instruction or at a target address of an identified branch instruction and ends just before another branch instruction...each of these microcode segments is individually compressed..." Craft disclosed compressing selective sections of code (asserting a signal). Also, Abstract, last line, "...the required memory for storing the compressed executable microcode is reduced.")

-OR means for asserting and outputting the uncompressed data selection signal when at least one of the branch instruction detection signal from said branch instruction determination means and the section trace start signal from said event management means is active.

Swoboda discloses a trace facility, but failed to disclose details on compression and an active / inactive signal. However, Craft disclosed (Col. 3, lines 25-42, "...an address location of each branch instruction within this set of compiled microcode may be identified...This set of compiled microcode is then parsed into some number of microcode segments...Each of these microcode segments begins after an identified branch instruction of at a target address of an identified branch instruction and ends just before another branch instruction. Subsequently, each of these microcode segments is individually compressed by utilizing a data compressing routine...All the individual compressed microcode segments are concatenated together with the uncompressed branch instruction to yield a compressed executable microcode image...the compressed segments comprising executable microcode image are linked by inserting the correct target address within each branch instruction in its uncompressed form..." Craft compresses code, a signal is asserted at selection detection. Craft does not compress code if it is a branch instruction (signal to compress is not asserted).

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified Swoboda's invention to trace and detect branch addresses by including details as provided by Craft to selectively compress instructions because (Abstract, last line) "By doing so, the required memory for storing the compressed executable microcode is reduced." Resources are better used.

Per claim 5:

-frame address comparison means for asserting and outputting a frame match signal when the instruction address/instruction code contained in the event setting data output from said event setting means matches the trace memory address from said trace control means, (Swoboda allows for control conditions (col. 10, lines 42-43), "...bits that define control operations (frame match, event setting) available through controller card.", Col. 14, lines 2-6, "Analysis circuitry is connected to the CPU core...includes condition sensors such as hardware breakpoint sensors for controlled stops and trace stack circuitry for real-time trace recordkeeping...")

-said OR means asserts and outputs the uncompressed data selection signal when at least one of the branch instruction detection signal from said branch instruction determination means, the section trace start signal from said event detection means, and the frame match signal from said frame address comparison means is active.

Swoboda discloses a trace facility, but failed to disclose details on compression and an active / inactive signal. However, Craft disclosed that some instructions/data code are to remain uncompressed. The type of instruction is detected and a decision is made, and signal asserted, whether to compress or not.

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified Swoboda's invention to trace and detect branch addresses by including details as provided by Craft to selectively compress instructions because (Abstract, last

line) "By doing so, the required memory for storing the compressed executable microcode is reduced." Resources are better used.

Per claim 6:

-a trace memory for compressing and storing an instruction address that has traced a program; (Swoboda: Abstract, last sentence, "...pushing the jump address (instruction address) onto a trace stack (storing).")

Swoboda discloses a trace facility, but failed to disclose details on compression. However, Craft disclosed that some instructions/data code is compressed. The type of instruction is detected and a decision is made, and signal asserted, whether to compress or not. See Craft, Abstract, lines 7-12, "...each microcode segment begins at an instruction following each identified branch instruction of at a target address of each identified branch instruction...individually translated to its compressed form..."

-event detection means for, upon detecting one of a preset predetermined instruction address and predetermined instruction code, controlling to write an instruction address, in which one of the predetermined instruction address and predetermined instruction code is stored, in said trace memory as uncompressed data.

Swoboda discloses a trace facility, but failed to disclose details on compression. However, Craft disclosed that some instructions/data code is compressed, while some is left uncompressed.

See Fig. 2, #25, "Insert address of branch locations for compressed microcode." Col. 3, lines 38-42, "All the individual compressed microcode segments are concatenated together with the uncompressed branch instructions to yield a compressed executable microcode image...Finally the compressed segments comprising executable microcode image are linked by inserting the correct target address within each branch instruction in its uncompressed form..."

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified Swoboda's invention to trace and detect branch addresses by including details as provided by Craft to selectively compress instructions because (Abstract, last line) "By doing so, the required memory for storing the compressed executable microcode is reduced." Resources are better used.

Conclusion

10. Japanese patents supplied as IDS appear to be relevant to the rejections of claims 1-6, but English translations are not available.

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Steelman, whose telephone number is (703) 305-4564. The examiner can normally be reached Monday through Thursday, from 7:00 A.M. to 5:30 P.M. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on (703) 305-4552.

The fax phone number is (703) 872-9306 for regular communications and for After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Mary Steelman

04/15/2004

ANTONY NGUYEN-BA
PRIMARY EXAMINER